IN THE DRAWINGS:

Please substitute the attached Replacement Sheet(s) for its(their) corresponding drawing sheet(s) in this Application.

REMARKS

Applicant appreciates the time taken by the Examiner to review Applicant's present application. This application has been carefully reviewed in light of the Official Action mailed March 24, 2004. Applicant respectfully requests reconsideration and favorable action in this case.

Claims 1-24 and 27-28 and 30 are pending in this application. Claim 30 is newly presented. Claims 25-26 and 29 are cancelled without prejudice or disclaimer.

Claims 1-5, 7, 9-14, 17-18 and 27-28 are amended to more clearly define the invention. Claims 6, 8, 15-16 and 19-22 are rewritten in independent form and are, therefore, not narrowed. Support for the important limitation of the multiple timing signals that are different in frequency, phase or both frequency and phase is found in figures 3 and 7, and claim 5 as originally filed. Support for new claim 30 is found in claim 27 as originally filed. Support for the recitation of a digital phase detector in claims 18 and 19 is found in figure 5 and the paragraph bridging pages 19-20 of this application as originally filed. claim 18 as originally filed. Support for the recitation of a digital phase-frequency detector in claim 19 is found in claim 18 as originally filed.

The title is amended to more concisely name the claimed invention. The abstract is amended to more accurately summarize the claimed invention. The specification is amended to more clearly describe the invention.

Applicant submits herewith one copy of eight sheet(s) of replacement drawings. Applicant requests that the Examiner approve the substitute drawings. Marked-up versions of the substitute sheet(s) of drawings are attached hereto with the change(s) shown with red ink markings. Support for the depiction of detail number 86 in figure 5 is found at line 10 of page 22 of this application as originally filed.

At page 2 of the Office Action, the Examiner makes the restriction requirement final. As noted above, claims 25-26 and 29 are cancelled without prejudice or disclaimer.

Claims 1-5, 9-12, 14, 17-18 and 28 were rejected under 35 USC 102(b) as anticipated by DaSilva (i.e., U.S. Patent No. 5,105,168). The disclosure of DaSilva is not sufficient to support this rejection.

DaSilva teaches "[a] vector locked loop is disclosed having a topology somewhat similar to two cross coupled phase locked loops, but wherein both magnitude and phase are used as feedback signals. The output signal of DaSilva is generated by combining the outputs of two VCOs in a combiner network. This output signal is fed back to the input, where phase and magnitude detectors are used to generate error signals. These error signals are processed by DaSilva to yield control signals for controlling the frequencies of the two VCOs.

DaSilva only cites a specific configuration which employs ***pairs*** of VCOs which both operate at similar carrier frequencies (separated only by the modulation frequencies); in the claimed invention, the disclosed system configuration permits ***any number*** of separate oscillators (VCOs), even down to one, each operating individually and not in any way required to operate as cross-coupled pairs.

In DaSilva the two VCOs are combined to produce the single composite output signal. In the claimed invention, the required VCOs have individual outputs (***and*** at different frequencies).

The claimed invention is concerned with receiver synchronization, whereas DaSilva never even mentions the topic of synchronization. In contrast to the claimed invention, DaSilva teaches a phase-locked signal generator that produces an amplitude/phase-modulated signal which closely emulates an input signal in both amplitude and phase.

The claimed invention is directed to a plurality of memory devices (of which a phase or phase/frequency detector *within a single PLL* is one example). The use by the Examiner in his response, item 4, of the entire vector lock loop (*dual* PLLs) of DaSilva as a memory device is a misconstruction of the clear exposition (explicit definition) of the phrase memory device as set

forth in this application as originally filed, where the memory device is described as a phase detector or phase-frequency detector (PFD) circuit, including the integrating capacitor (or equivalent) used to low-pass filter the error signal within the VCO control loop (please see figure 5 of the this application as originally filed). In Figure 5 of this application, cross-coupling signals are disclosed at both PFD inputs and into the integrating capacitor at the PFD output.

The claimed invention requires multiple timing signals. The Examiner has cited elements (64, 66) of DaSilva as "multiple timing signals", yet these are one and the same signal, **not** multiple signals. Further, the amplitude detector of DaSilva (his 38) has nothing to do with signal timing (phase), only its magnitude. Very clearly, each VCO in DaSilva has only one timing (phase) error signal [signal 42 applied through difference block 40 and filter 52 into VCO 1 (12), which is precisely the same signal as 58 [applied through summer block 54 and filter 62 into VCO 2 (14)]. Thus, in DaSilva, both VCOs are each fed a ***single*** timing signal (16 and 18 respectively), whereas in the claimed invention, each VCO's operating frequency is controlled by ***multiple*** (at least two) simultaneous timing signals developed from different sources [see Fig. 3 of the present case, where each CPFD-VCO combination (i.e., 31/34, 32/35, and 33/36) functions as a distinct PLL]. Further, DaSilva at no time discloses or suggests cross-coupling more than two VCOs, whereas this application as originally filed discloses methods of inter-locking an arbitrarily large number of diverse-frequency VCOs, so long as their frequencies are rationally related (either multiplied or divided by integer ratios).

With regard to claims 2, 7, 13, 14 and 28, the "common frequency reference source" may be at any one or more of the above frequencies, not necessarily that of any of the VCOs themselves (i.e., the reference could be at ¼ the frequency of the lowest-frequency PLL of the ensemble). In contrast, the "reference" (Input) of DaSilva may only be at the desired output frequency, except in the frequency-offset case with the mixer (please see DaSilva's figure 5).

With regard to claim 3, the Examiner has confused the intent of the claim, which simply describes the types of multiple external timing signals intended to be employed by the invention.

With regard to claims 13-14, 17-18 and 27, DaSilva does not disclose or suggest a phase-frequency detector, much less a composite or digital phase-frequency detector. Specifically, DiSilva's description of his figure 3 is limited to an analog difference circuit immediately following the phase detector (i.e., the loop of DiSilva as shown and desribed is totally analog.

Accordingly, withdrawal of this rejection is respectfully requested.

Claims 7, 13 and 27 were rejected under 35 USC 103 as obvious over DaSilva in view of Lee (i.e., U.S. Patent No. 5,568,078). The Lee reference does not obviate the above discussed deficiencies of DaSilva. Therefore, the disclosures of DaSilva and/or Lee alone,or in combination, are not sufficient to support this rejection.

In more detail, the teachings of the Lee reference are directed to dealing with duty cycle restrictions of phase detectors. Lee teaches duty cycle controllers that condition pulse widths so that conventional phase detectors operate correctly. Lee does not disclose or suggest multiple input timing signals, much less multiple input timing signals that are different in frequency. Lee takes only a single original input frequency from which Lee continually derives multiple frequencies at multiple outputs. In addition and with regard to claims 13-14, 17-18 and 27, neither Lee or DiSilva disclose or suggest any sort of composite phase-frequency detector.

Accordingly, withdrawal of this rejection is respectfully requested.

At page 1, item 7 and page 5 of the office action, the Examiner indicates that Claims 6, 8, 15-16 and 19-24 would be allowable if rewritten in independent form. This indication of allowable subject matter is very much appreciated. Claims 6, 8, 15-16 and 19-22 are rewritten in independent form and are, therefore, not narrowed. Claims 23-24 depend from Claim 22.

Other than as explicitly set forth above, this reply does not include acquiescence to statements in the Office Action. In view of the above, all the claims are considered patentable and allowance of all the claims is respectfully requested. The Examiner is invited to telephone

the undersigned (at direct line 512-394-0118) for prompt action in the event any issues remain that prevent the allowance of any pending claims.

In accordance with 37 CFR 1.136(a) pertaining to patent application processing fees, Applicant requests an extension of time from June 24, 2004 to September 24, 2004 in which to respond to the Office Action dated March 24, 2004. A notification of extension of time is filed herewith.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-3204 of John Bruckner PC.

Respectfully submitted,

John Bruckner PC
Attorney(s) for Applicant(s)

John J. Bruckner
Reg. No. 35,816

Dated: September 24, 2004

5708 Back Bay Lane
Austin, TX 78739-1723
Tel. (512) 394-0118
Fax. (512) 394-0119

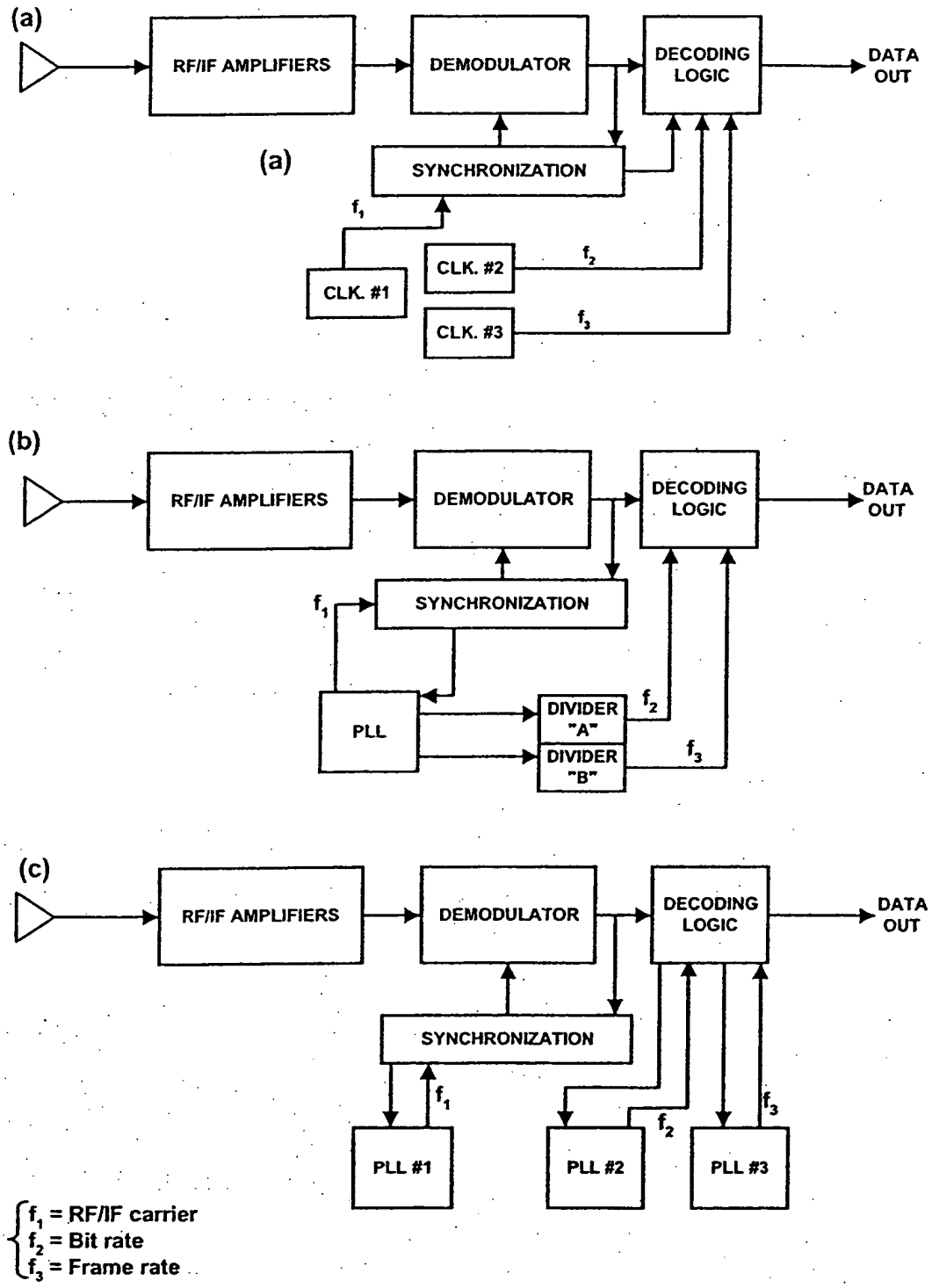


Fig. 1 [Prior Art]

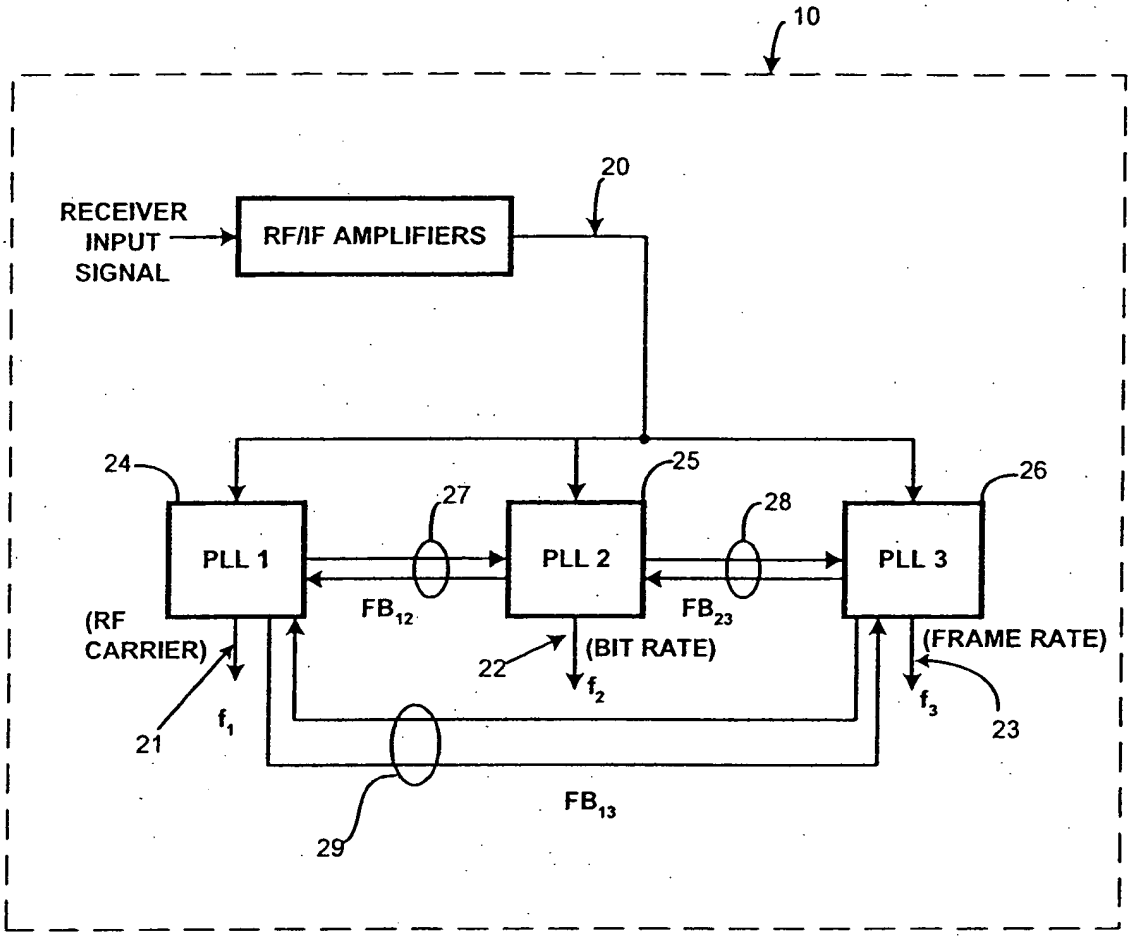

10
20
RECEIVER INPUT SIGNAL
RF/IF AMPLIFIERS
24
25
26
27
28
PLL 1
PLL 2
PLL 3
FB12
FB23
(RF CARRIER)
(BIT RATE)
(FRAME RATE)
22
21
f1
f2
f3
23
FB13
29

Fig. 2

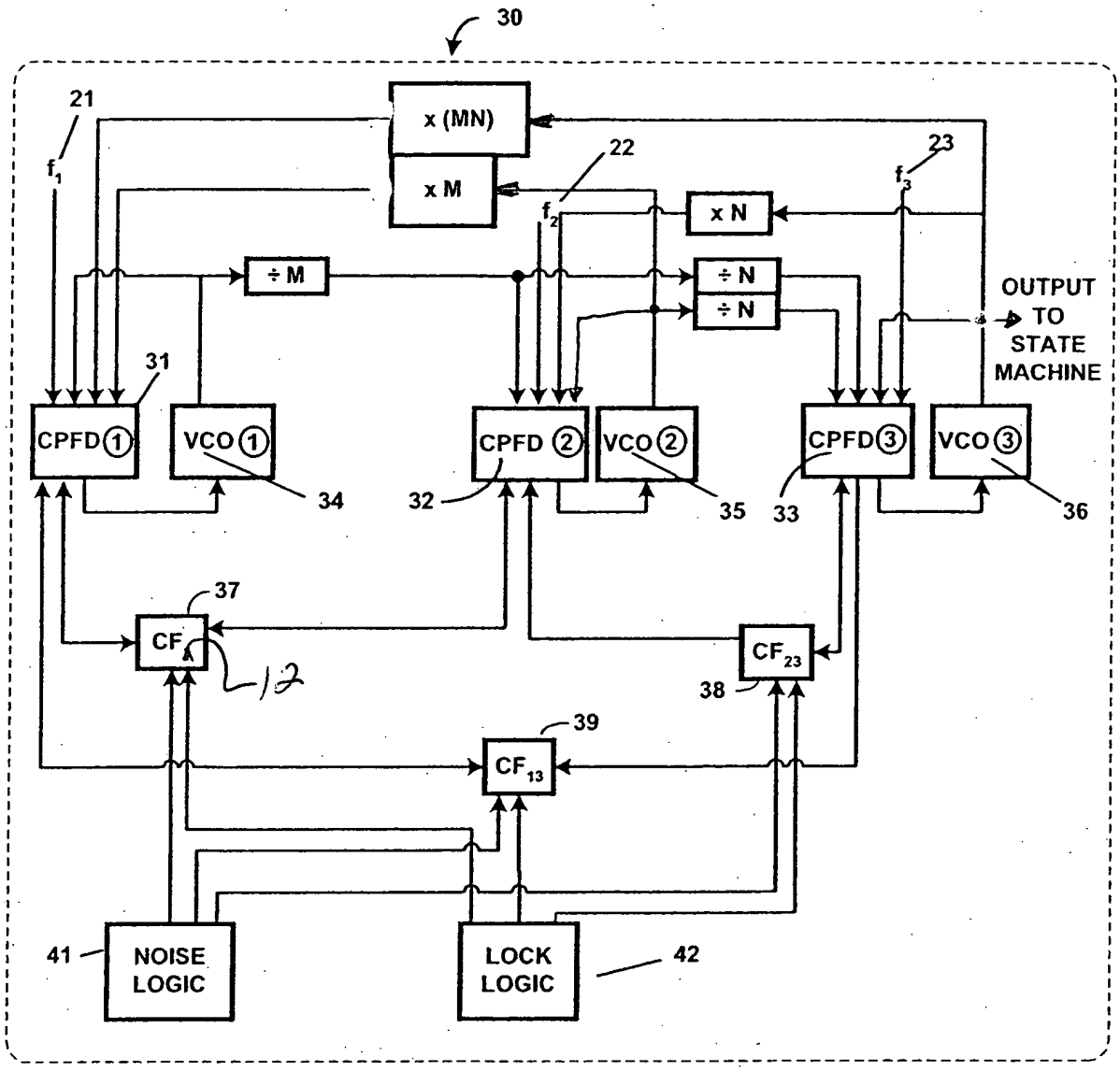
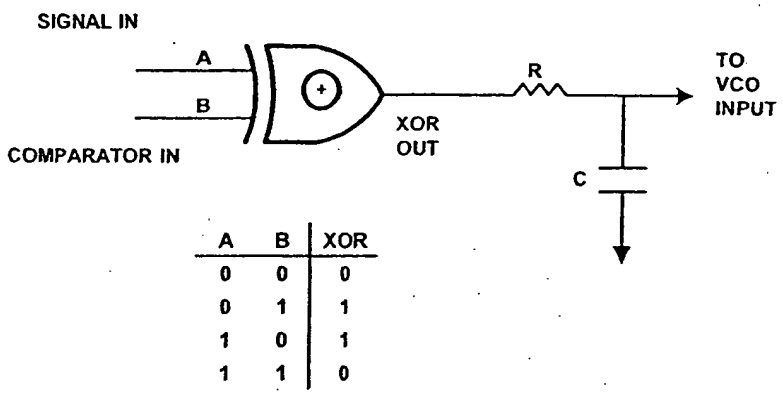
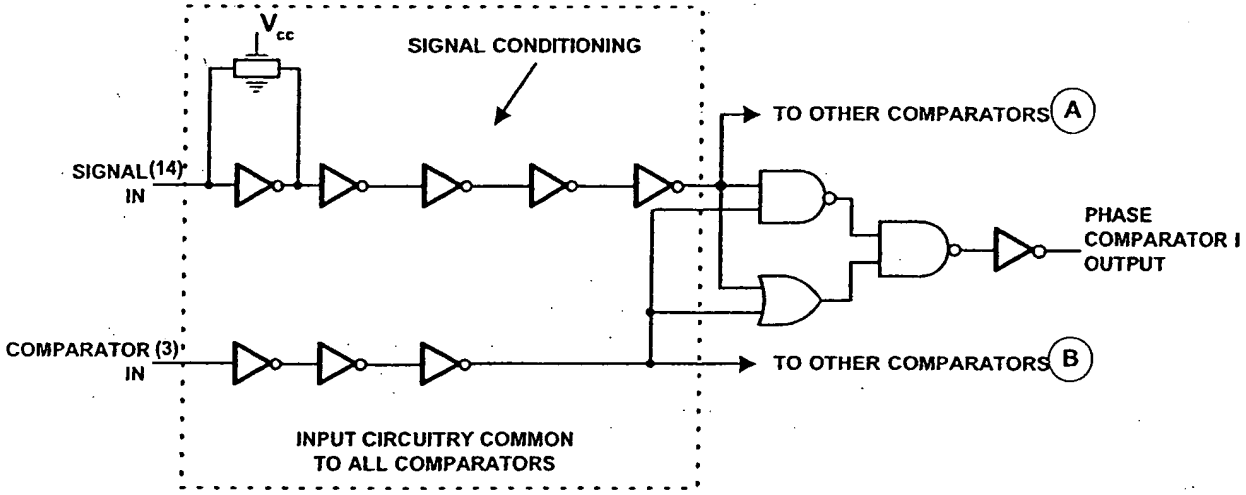


Fig. 3

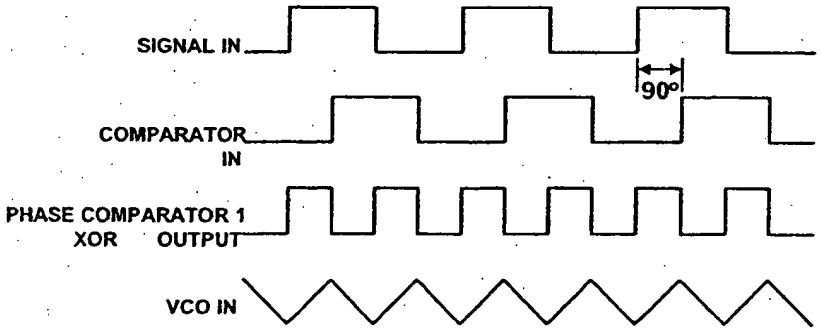


A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

(A) BASIC XOR PHASE COMPARATOR

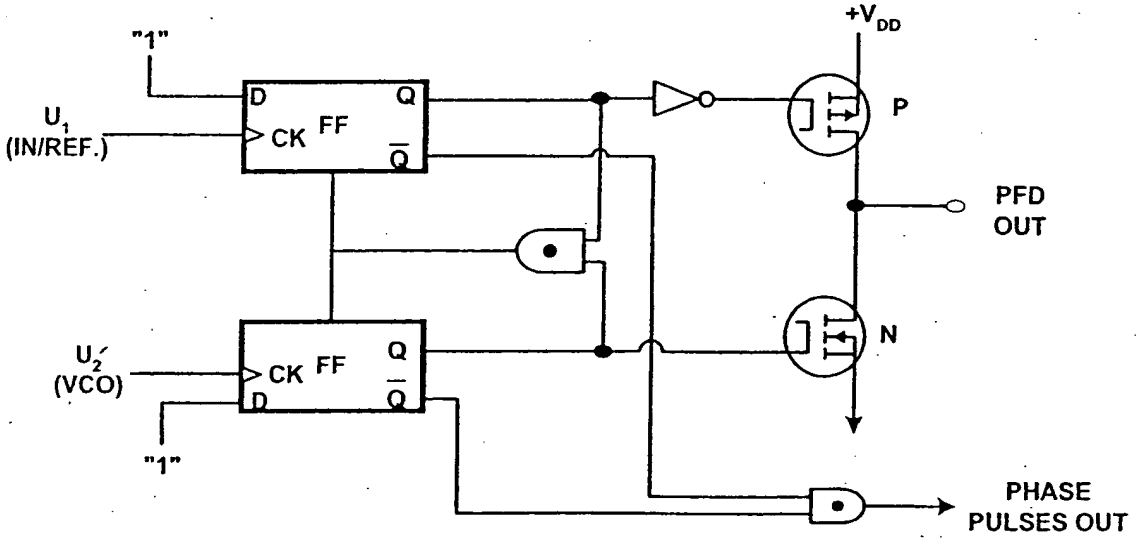


(B) DETAILED ON-CHIP IC CIRCUITRY IN 74HC4046

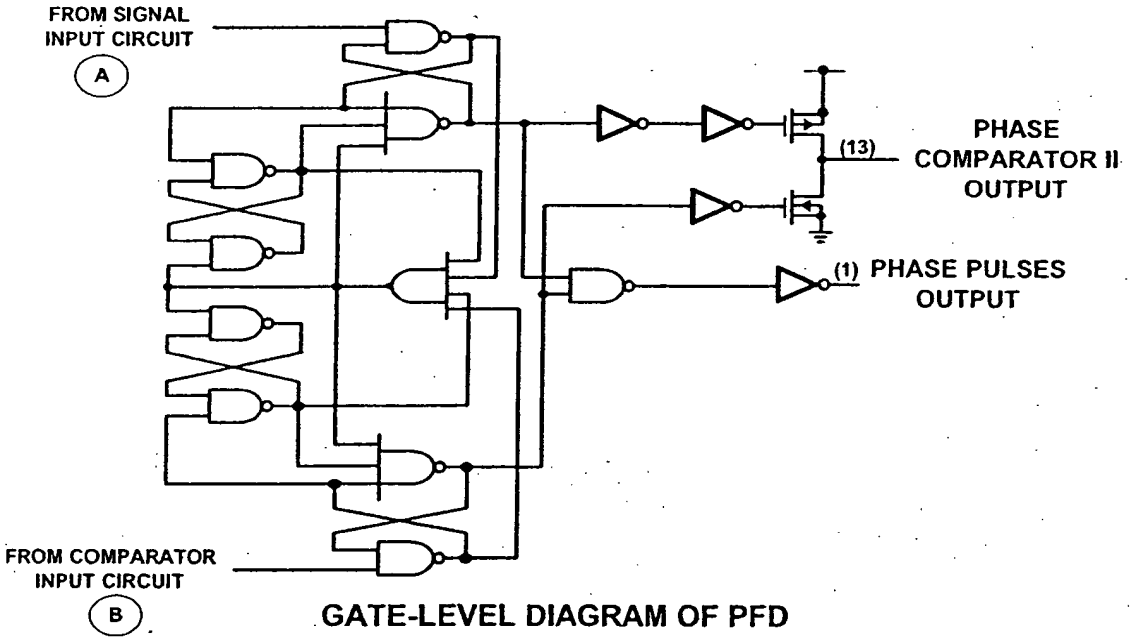


(C) TYPICAL XOR DETECTOR WAVEFORMS

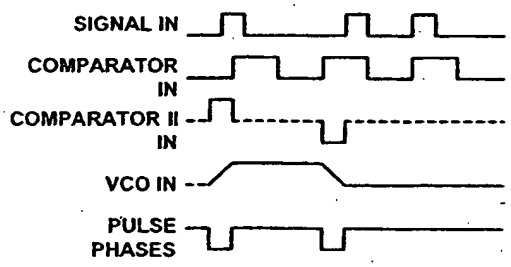
Fig. 4 (Prior Art)



HIGH-LEVEL DIAGRAM OF PFD (existing art)



GATE-LEVEL DIAGRAM OF PFD



TIMING AND WAVEFORMS OF PFD (existing art)

Fig. 4 cont. (Prior Art)

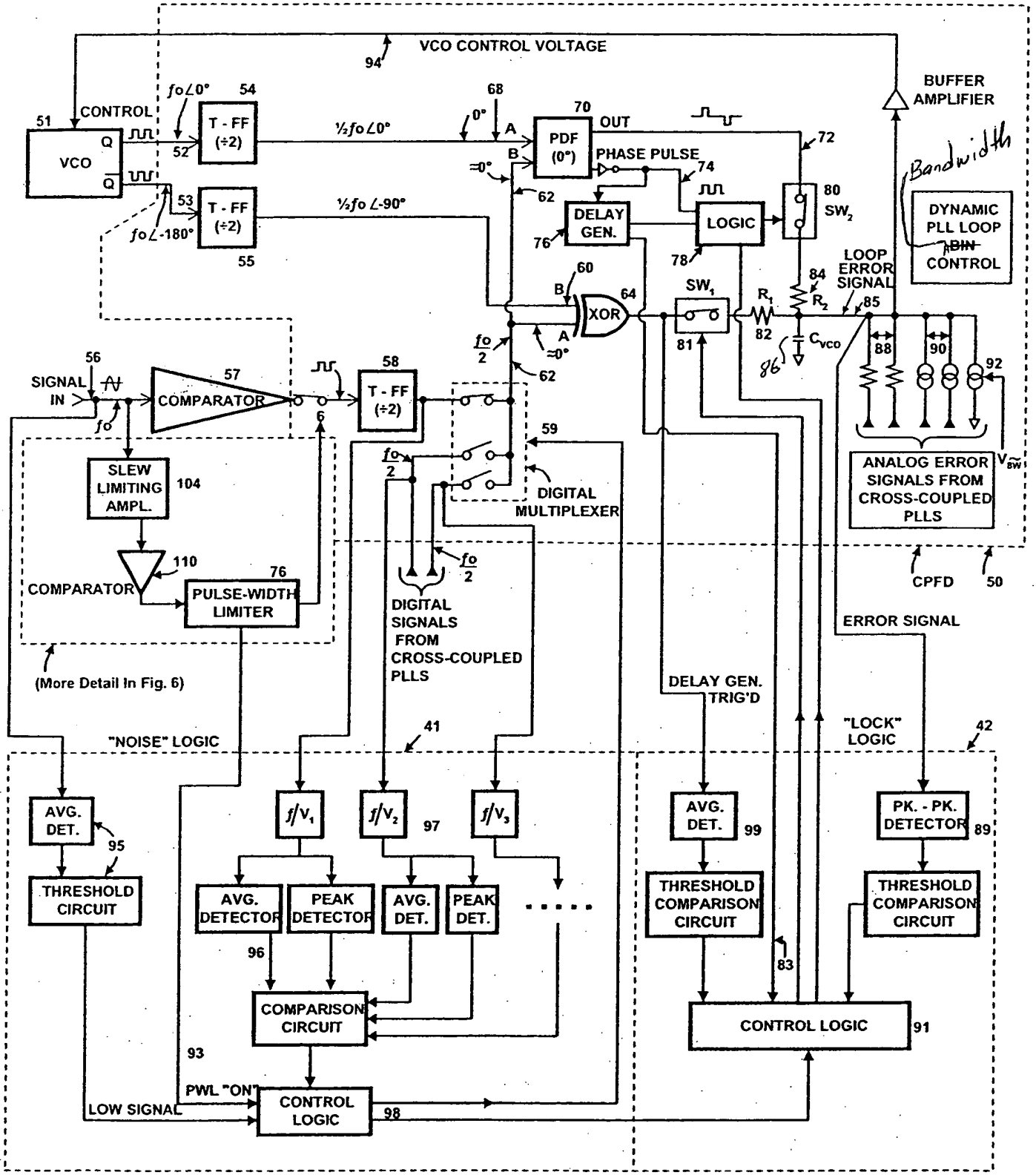


Fig. 5

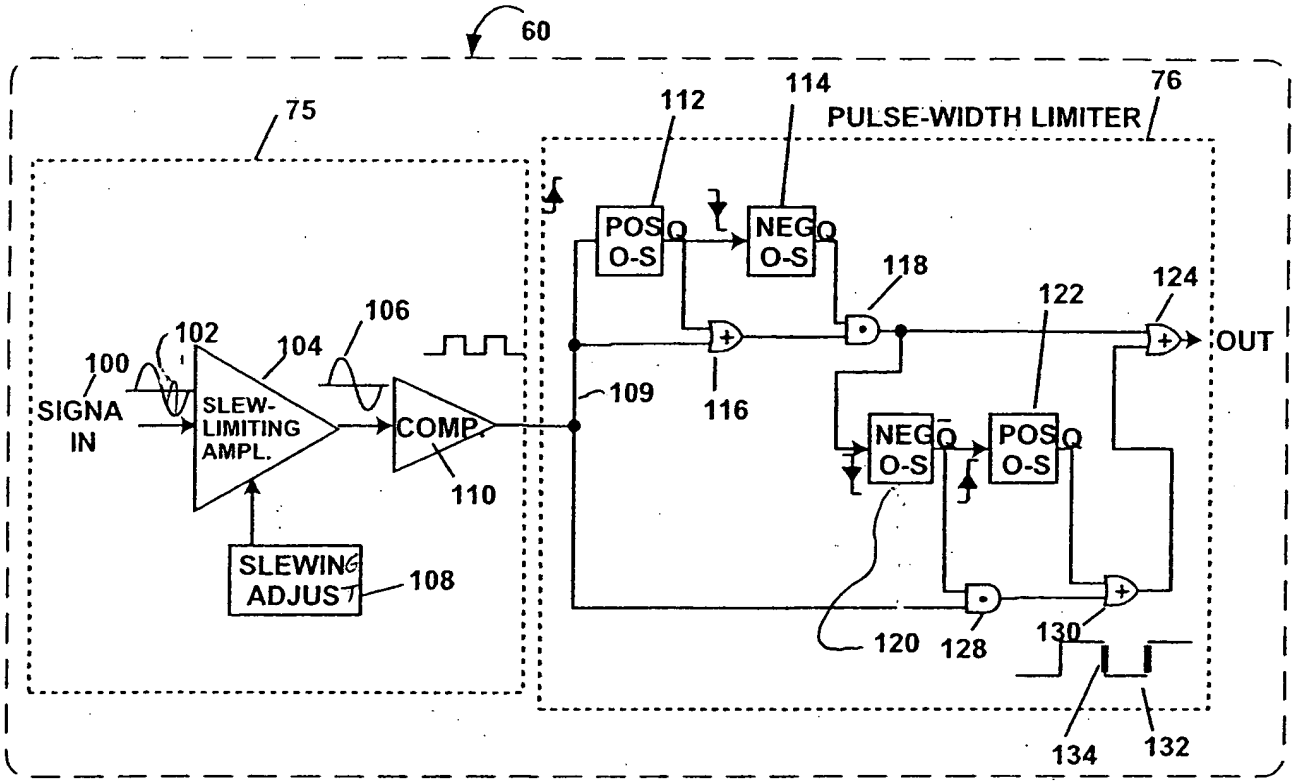


Fig. 6

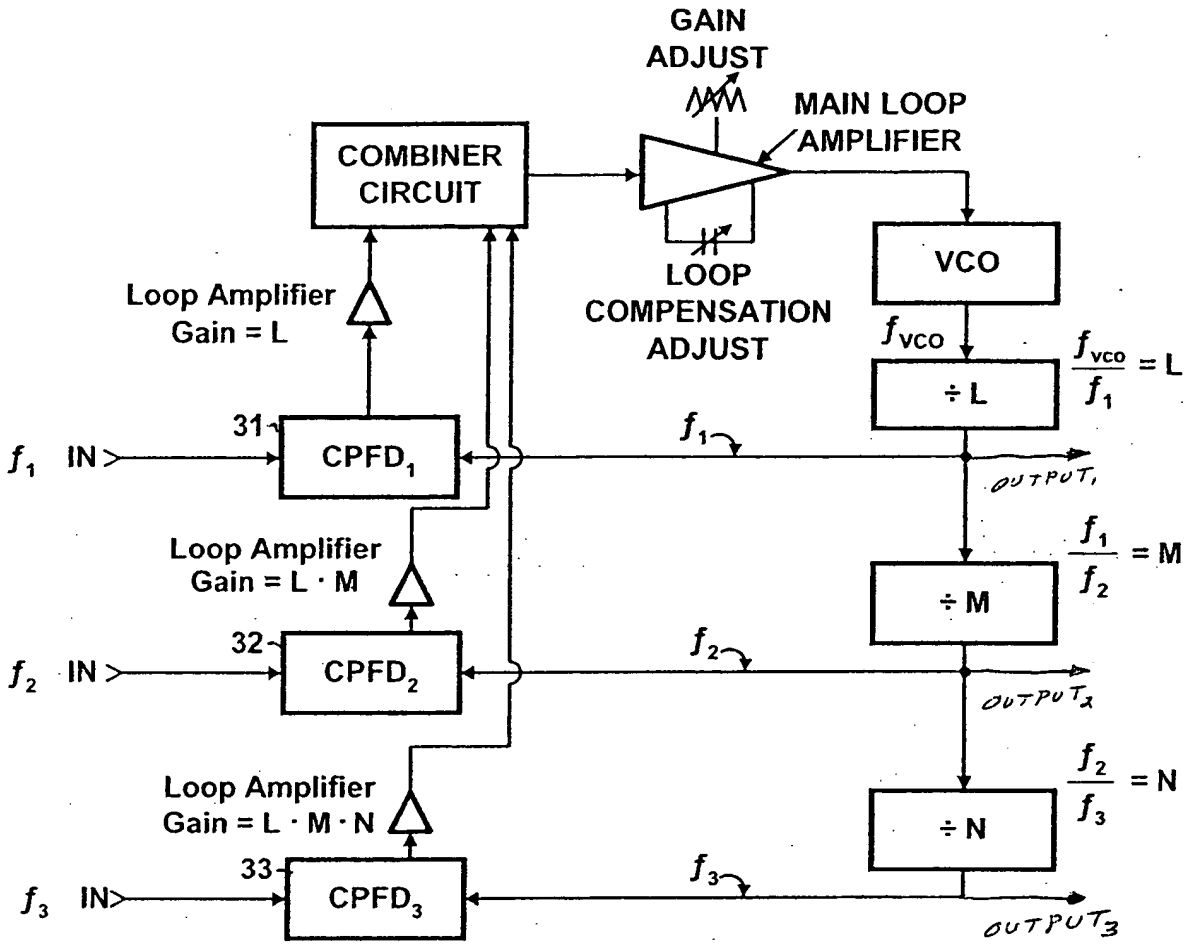


Fig. 7